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(71) Applicant *(for all designated States except US)*: N.V. PHILIPS' GLOEILAMPENFABRIEKEN [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)* : SCHOUTE, Frederik, Carel [NL/NL]; Orionlaan 94, NL-1223 AJ Hilversum (NL). AWATER, Geert, Arnout [NL/NL]; Oostsingel 17, NL-2612 HB Delft (NL).

(74) Agents: ROLFES, Johannes, Gerardus, Albertus et al.; Internationaal Octrooibureau B.V., Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

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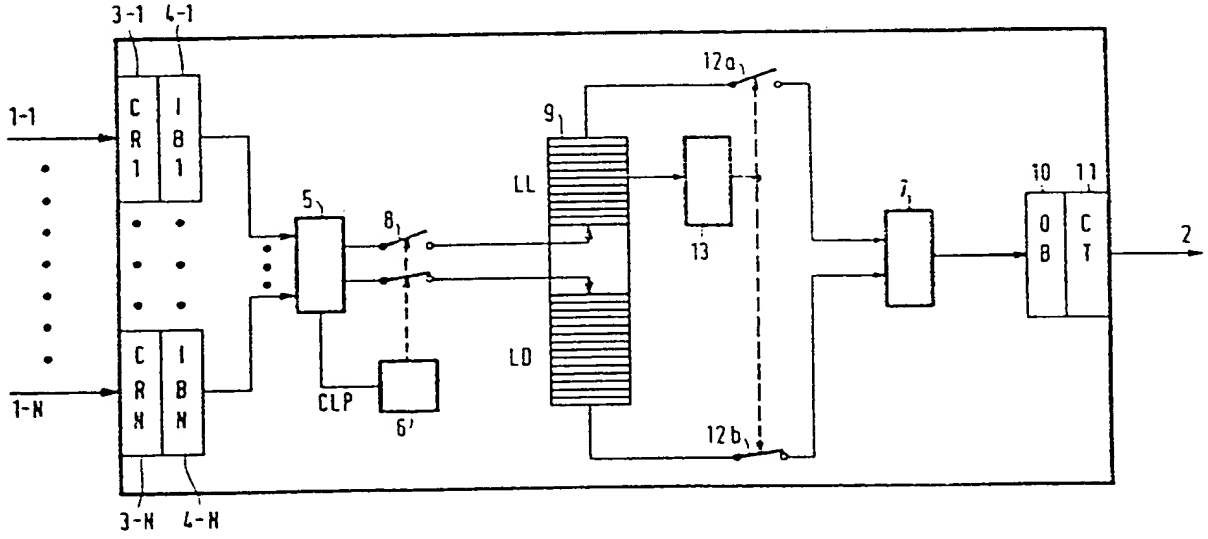

(57) Abstract

An ATM switching arrangement is disclosed in which two types of cells are distinguished. A first type of cells is marked as low loss and a second type of cells is marked as low delay. In the switching arrangement a cell buffer (9) is subdivided into a first memory area (LL) for the low loss cells and a second area (LD) for the low delay cells. In the case of the cell buffer (9) being completely filled, low loss cells get read-in priority over low delay cells. In reading out from the cell buffer low delay cells take priority over low loss cells, unless the low delay area is empty. It is also possible to set a threshold value for the content of the low loss area; when the content of the low loss area exceeds the threshold value, outputting of the low loss cells can then be started.

Low delay or low loss cell switch for ATM

The invention relates to a telecommunication switching arrangement for switching digital data which are contained in data cells provided with a cell header, the arrangement comprising a crosspoint switch for switching cells from an input line of the switch to an output line of the switch, the switch being provided with a cell buffer memory for storing the cells to be switched through.

Such an arrangement can be used for fast packet switching techniques which are known under the name of ATM (Asynchronous Transfer Mode). The power of ATM is its ability to provide bandwidth on demand: different sources can have different bandwidth requirements.

Fast packet switching techniques clearly provide the flexibility for integration of mixed traffic streams, such as voice, data and video. Due to provision for the stochastic bandwidth requirements of some traffic sources, it is not so clear at first sight whether a reasonable degree of utilization of switching and transmission resources can be achieved. That is, the primary benefit of fast packet switching lies in its flexibility to serve different traffic streams. The invention has for its object to provide an ATM system that can serve different types of traffic streams and which also uses capacity more efficiently than known arrangements.

Thereto, according to the invention, the switching arrangement is characterized in that:

- the cell buffer memory consists of at least two memory areas, one area called the low loss area and the other area called the low delay area,
- the crosspoint switch is further provided with an evaluation circuit for determining the value of a predetermined bit in the cell header, the evaluation circuit producing an evaluation output signal dependent on the determined value.

- the crosspoint switch is provided with allocation means receiving the evaluation output signal, for allocating incoming cells to the low loss area or to the low delay area in dependence on the value of the evaluation output signal.

The invention makes use of the insight that some sources require low delay variation whereas other sources require low loss probabilities for ATM cells. From the CCITT Draft Recommendation I.361: "ATM layer specification for B-ISDN", January 1990, it is known that the ATM cell header should have a Cell Loss Priority (CLP) bit. This CLP bit creates the possibility to distinguish between two types of cells.

The performance of the ATM network as exposed to the user, depends primarily on the call acceptance probability. Known methods of resource allocation usually decide to accept an ATM connection if the resulting cell loss probability for of the aggregate input traffic remains below a preset maximum value. In these known methods the expected cell delay is considered of minor importance. Sometimes a higher cell loss probability can be tolerated, which then could be specified in the cell header, e.g. by using the CLP bit. Hereby two classes of traffic are introduced. The first class encompasses traffic requiring low loss probability. Traffic of the other class gives in on loss probability but gets a lower delay variation in return.

Sources that generate traffic whose time relation needs to be restored after passage through the asynchronous transfer network , benefit from a low delay variance. This is so since delay dejitter buffers in the terminal equipment can be kept smaller if the trans-network delay variance is small. Traffic sources that generate traffic for which the integrity is of prime importance, on the other hand, will prefer a low probability of cell loss. An example of the latter is (machine oriented) data traffic, an example of the first is (human oriented) audio/visual traffic.

With integrated circuit technology one can realize buffers for several hundreds of ATM cells on one chip. These buffers, together with on-chip control logic, can be used to implement LDOLL (Low Delay Or Low Loss) queues. An LDOLL queuing policy favours low delay cells in service priority and low loss cells in storage priority.

To describe the sources of different traffic streams it should be realized that a cell transmission takes a few micro-seconds, a burst of cells (activity period of a source) lasts,

say, a fraction of a second, and the connection between source and destination can stand for a several minutes.

Connections do not always need the full bandwidth for the whole duration of the connection. Moreover, the bandwidth requirement usually differs for the go or return path of a connection. Some traffic sources like some video coders have a variable bit rate (VBR). E.g. in the case of a file transfer, a burst of packets is transmitted. Termination of the file transfer does not necessarily imply immediate termination of the connection because more data may be exchanged subsequently. In the case of a VBR coder, the cell rate (i.e. bandwidth) may change every 1/25 s. (resp. 1/30 s.), once every video frame. With its cell buffer array the LDOLL queue can allow for short periods of overload. This could provide an alternative for burst blocking.

The invention will be further explained in the following with reference to the drawing Figures, in which:

Figure 1 shows an embodiment of an ATM switching arrangement according to the invention;

Figure 2 shows a graphical representation of the probability of loss of LD and LL cells of the switching element according to the invention, compared with a FIFO policy;

Figure 3 shows a graphical representation of the delay of LL and LD cells compared with cell delay in a FIFO read-out policy;

Figure 4 shows a graphical representation of the probability of LL and LD cell loss compared with a FIFO policy, dependent on a threshold value;

Figure 5 shows a graphical representation of the cell delay of LL and Ld cells compared with a FIFO policy, dependent on a threshold value.

Fig. 1 shows an ATM switching arrangement which might be considered the elementary building block of an ATM network. The arrangement has N ATM input links 1-1 through 1-N and one ATM output link 2. It is assumed that all links of the switching arrangement operate synchronously; the interval between two successive (idle) cell arrivals is called a time slot.

The cell receivers 3-1 through 3-N deserialize an incoming cell and store it after

complete reception into input buffers 4-1 through 4-N. Deserialization makes it possible to examine the header information, and to process ATM cells in parallel. This allows practical switching elements to cope with the high switching speeds (millions of cells per second). Cell queuing element 5 receives the ATM cells from the input buffers. This cell queuing element can be implemented as a well-known elastic read-write buffer. It transfers the non-empty cells from the input buffers to the cell buffer array 6.

Cell queuing element 5 can also evaluate the value of the CLP bit in the cell header. This value is transferred to a switch actuator 6 which controls the opening and closing of a pair of switches 8. The cell to be transferred to the cell buffer will thereby be placed in the LL part of the cell buffer or in the LD part, depending on the value of the CLP bit.

The cells are transferred from the input buffers to the cell buffer array 6 with storage priority for LL cells. That is, when the cell buffer array is full, an LL cell present at an input buffer will (under control of switch actuator 6) replace the oldest LD cell in the cell buffer array. By replacing the oldest LD cell the average delay for LD cells is minimised. LL cells are lost only due to blocking when the cell buffer array is completely filled with LL cells. LD cells are lost due to replacement or blocking when the cell buffer array is full.

The cells in the buffer array are organised in two linked lists: one list to comprise all low delay (LD) cells (the low delay area LD), the other for all low loss (LL) cells (the low loss area LL). For each type the oldest cell is always at the head of the list.

Cell server 7 takes cells out of the cell buffer 9; the type of cells to be read out depends on the number of LL cells and LD cells in the cell buffer. In this service policy a threshold TH (which f.i. has a value 40) is used, which means that LD cells are served first as long as less than 40 LL cells are in the cell buffer array 9. The decision which type of cell should be read out is taken by a monitoring circuit 13, which monitors the number of cells in the low loss area of the cell buffer. If number of cells in LL exceeds the (adjustable) threshold TH, a switch pair 12a, 12b is actuated whereby reading of cells from the LD area is stopped and reading of cells from the LL area is started.

The output buffer transfer cells to the cell transmitter 11 which serializes it and puts them onto its outgoing link 2. Every time slot, cell service takes place prior to the enqueuing of a new cell into the cell buffer.

The cell server could optionally bypass the cell enqueuer and the cell buffer. This situation occurs for example, if the cell server finds the cell array 9 empty, and the input buffers hold at least one cell. It must be noted that, even if cells were transferred from the input to the output buffers infinitely fast, the (de)serialization of cells, introduces a delay of one time slot, i.e. the time needed for transmission of an entire cell. However, if it is assumed that enqueuing and subsequent serving takes a single time slot or more, the minimal delay introduced by the switching arrangement is two time slots.

In figures 2 through 9 results are shown of calculations and simulations that have been carried out to investigate the properties of the switching element of figure 1. In this simulation attention has been paid to variations in source activity and especially interesting is the case where temporary overload occurs. A switching element having two inputs has been assumed. It is also assumed that the LDOLL queue feeds a transmission outlet with a capacity of 150 Mbit/s. The cell size was assumed to be 53 octets, with a payload of 44 octets. A number of connections is multiplexed on each input channel. One channel carries the combined output streams of a number of VBR coders, with an average bit rate of 3.9 Mbit/s. The other channel carries traffic produced by a number of on/off sources (e.g. file servers), with a peak band width of 3 Mbit/s and an average on-time and off-time of 0.1 s.The VBR output stream consists of 90% LD cells and 10% LL cells. For the on-off traffic the reverse ratio is assumed. Each 1/30-th second, the bits of one frame are packed into cells which are transmitted at a constant average rate.

The simulation of the LDOLL queue is carried out with a cell buffer size of 50 buffers and a threshold value TH of 40 and with a varying number of traffic sources. The numbers of on-off and VBR sources were chosen the same, so that the LD load was about 2/3 of the total load. By varying the numbers of both sources from 19 to 23 the total load applied to the LDOLL queue could be varied.

Figure 2 shows the probability of loss of LD (dashed line) and LL cells (unbroken line) of the switching element according to the invention, compared with a FIFO (first-in, first-out) way of outputting cells from the cell buffer (dotted line). The cell loss probability is shown in this figure as a function of the loading. The cell loss that would occur if conventional FIFO queuing were used, is almost entirely inflicted on the LD cells; the

average LL cell loss probability is greatly reduced. This remains true even if the loading approaches unity. Then the LD cell loss probability becomes 1, since because of the storage priority the buffer as sen by LL cells is virtually empty. Figure 2 shows that in case of buffer overload the LD cells, by the replacement mechanism, are the first ones to be discarded.

In figure 3 the delay of LL cells (dashed line) and of LD cells (unbroken line) and are compared with cell delay in a FIFO read-out policy (dotted line). The cell delay is shown in this figure as a function of the loading. This figure shows that, compared with a FIFO policy, the delay of LD cells is significantly reduced at the expense of a higher delay of LL cells.

Figure 4 shows the probability of LL and LD cell loss compared with a FIFO policy, dependent on the threshold value TH. It appears that the LD loss probability is relatively insensitive to changes in the value TH.

Figure 5 illustrates the cell delay of LL and Ld cells compared with a FIFO policy, dependent on the threshold value TH. Increasing TH lessens the average delay for LD cells and increases the average LL cell delay, at the same time increasing the loss rate of LL cells. With this scenario there is no TH that yields an LD cell delay larger than that for LL cells.

Claims:

1. Telecommunication switching arrangement for switching digital data which are contained in data cells provided with a cell header, the arrangement comprising a crosspoint switch for switching cells from an input line of the switch (1-1; 1-N) to an output line (2) of the switch, the switch being provided with a cell buffer memory for storing the cells to be switched through,

characterized in that:

* the cell buffer memory consists of at least two memory areas, one area called the low loss area and the other area called the low delay area,
* the crosspoint switch is further provided with an evaluation circuit for determining the value of a predetermined bit in the cell header, the evaluation circuit producing an evaluation output signal dependent on the determined value,
* the crosspoint switch is provided with allocation means receiving the evaluation output signal, for allocating incoming cells to the low loss area or to the low delay area in dependence on the value of the evaluation output signal.

2. A telecommunication switching arrangement as claimed in claim 1, provided with read out means for reading the cells from the cell buffer memory, which means are arranged for monitoring the number of cells in the low loss area and for switching over to reading cells from the low loss area if a predetermined threshold value of that cell number is exceeded.

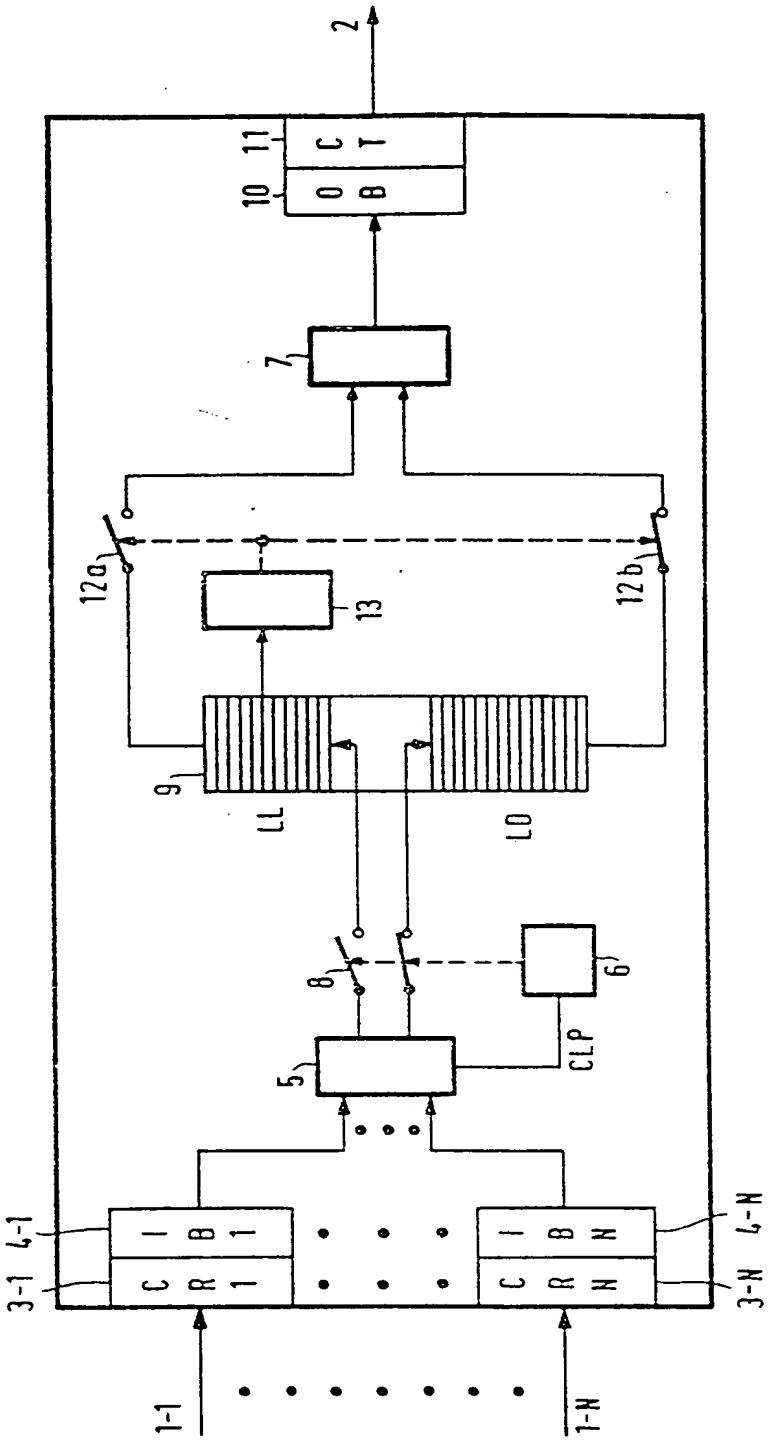
2
11
10
C T
O B
7
12a
12b
13
9
LL
LO
8
6
CLP
5
3-1
4-1
C R 1
I B 1
C R N
I B N
3-N
4-N
1-1
1-N

FIG.1

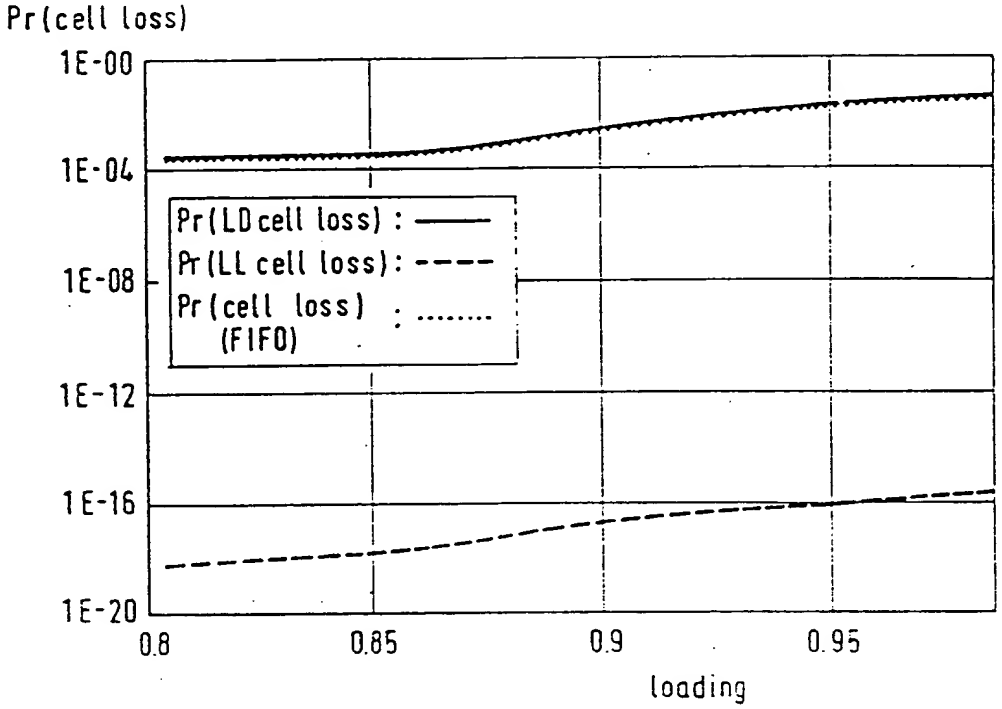
Pr(cell loss)
1E-00
1E-04
1E-08
1E-12
1E-16
1E-20
Pr(LD cell loss) :
Pr(LL cell loss) :
Pr(cell loss) (FIFO) :
0.8
0.85
0.9
0.95
loading

FIG.2

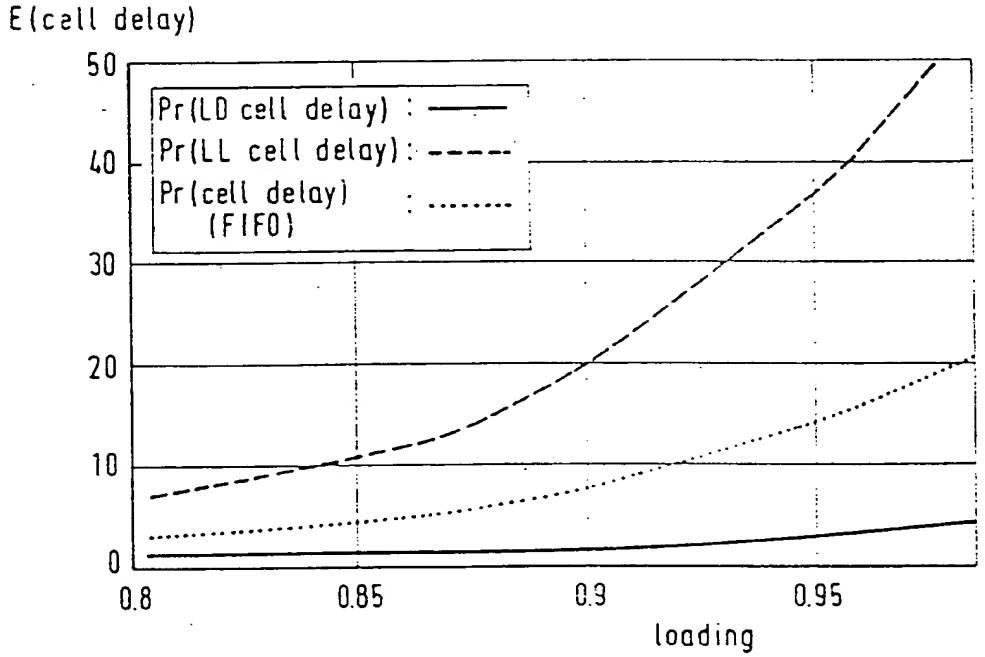
E(cell delay)
50
40
30
20
10
0
Pr(LD cell delay) :
Pr(LL cell delay) :
Pr(cell delay) (FIFO) :
0.8
0.85
0.9
0.95
loading

FIG.3

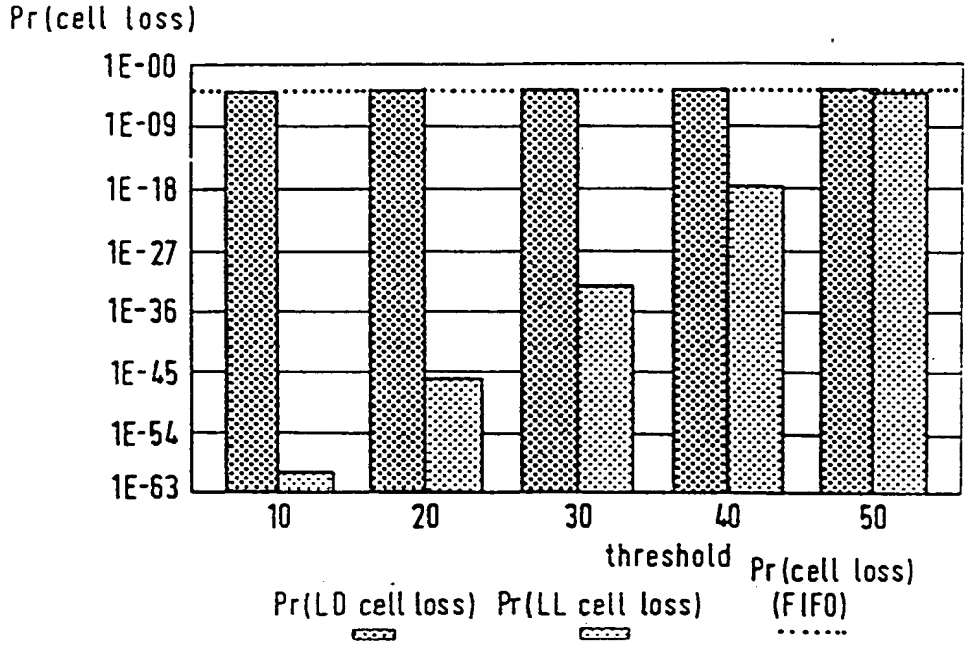
Pr(cell loss)
1E-00
1E-09
1E-18
1E-27
1E-36
1E-45
1E-54
1E-63
10
20
30
40
50
threshold
Pr(LD cell loss)
Pr(LL cell loss)
Pr(cell loss) (FIFO)

FIG.4

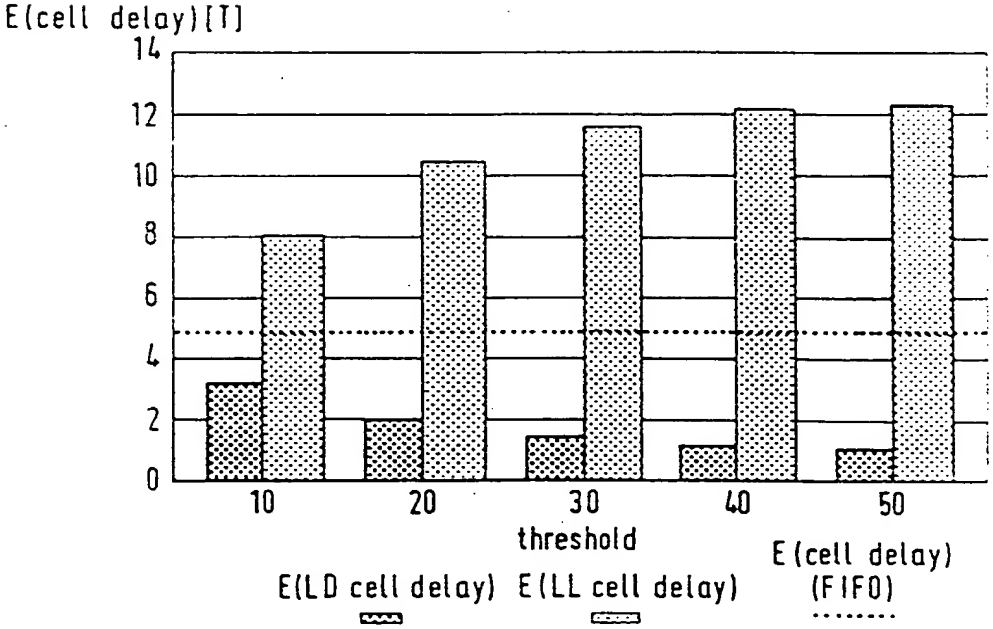
E(cell delay)[T]
14
12
10
8
6
4
2
0
10
20
30
40
50
threshold
E(LD cell delay)
E(LL cell delay)
E(cell delay) (FIFO)

FIG.5

INTERNATIONAL SEARCH REPORT

International Application No PCT/NL 92/00067

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 H04L12/56

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	H04L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document,[11] with Indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
X	EP,A,0 407 161 (KABUSHIKI KAISHA TOSHIBA) 9 January 1991 see column 2, line 24 - column 3, line 2 see column 3, line 16 - line 40	1
Y	---	2
Y	PROCEEDINGS OF THE IEEE vol. 79, no. 2, February 1991, NEW YORK, US pages 170 - 189; J. BAE ET AL: 'SURVEY OF TRAFFIC CONTROL SCHEMES AND PROTOCOLS IN ATM NETWORKS' see SECTION VA, PARAGRAPHS 2 AND 3	2

X	INT. SWITCHING SYMPOSIUM 90 vol. 5, May 1990, STOCKHOLM, SE pages 21 - 26; T. KOINUMA ET AL: 'AN ATM SWITCHING SYSTEM BASED ON A DISTRIBUTED CONTROL ARCHITECTURE' see SECTION 5.2.4	1

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
23 JULY 1992	17.08.92

International Searching Authority	Signature of Authorized Officer
EUROPEAN PATENT OFFICE	ALI A.

Form PCT/ISA/210 (second sheet) (January 1985)

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category °	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
A	EP,A,0 362 723 (PHILIPS VERWALTUNG) 11 April 1990 see column 3, line 28 - line 42	1,2
A	IEEE JOURNAL ON SELECTED AREAS IN COMMUNICATIONS vol. 6, no. 9, December 1988, NEW YORK, US pages 1609 - 1616; H. OHNISHI ET AL: 'FLOW CONTROL SCHEMES AND DELAY/LOSS TRADEOFF IN ATM NETWORKS' see SECTION IIIC	2

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO.

NL 9200067
SA 59181

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
The members are as contained in the European Patent Office EDP file on
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23/07/92

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		JP-A-	3113935	15-05-91
EP-A-0362723	11-04-90	DE-A-	3833490	05-04-90
		JP-A-	2143747	01-06-90
		US-A-	5067124	19-11-91